Design of Power Gated True Single-Phase-Clocked Flip-Flop

Pratiman Singh, Dr. Prashant K.Shah[1]

Dept of ECE, College of SVNIT, Surat, Gujarat

DOI:10.37648/ijrst.v12i03.002

Received: 11 May 2022; Accepted: 03 July 2022; Published: 04 July 2022

ABSTRACT

In low-voltage functions, power optimization is critical. This paper shows how to make a low-power Data -Flip flop circuit with header power gating. The architecture's main purpose is to investigate D Flip flop power dissipation in the conceptual design style. Tanner EDA is used to carry out the planned design. The simulation results reveal that using power gating, our suggested cell consumes significantly less energy.

Keywords—*Power gating, D Flip flop, Low voltage applications.*

INTRODUCTION

Mostly in design of integrated circuits, power consumption is a crucial concern. Large heat dissipation has a negative impact on performance and reliability. Another reason to limit power dissipation is to make the battery last longer. Digital circuitry makes extensive use of D flip-flops. Its power dissipation is minimized, resulting in a significant reduction in overall power consumption.

The advancement of low-power nanotechnology circuits is required by the growing demand for transportable, rechargeable batteries electronics devices (including such mobile personal digital assistants (pdas). The difficulty of delivering power dissipation may limit the functionality of computing systems as the density and complexity of processors continues to expand. Power dissipation, in particular, consumes around 35% of the chip's power at the nanoscale level.

The goal of this research is to examine the performance of Power Gating, which is one of the most reliable ways to low-power design. The emphasis is solely on nanometer-scale CMOS devices, as this is the most widely used technology in today's VLSI systems. A circuit can function in two modes when using the power gating arrangement. Sleep transistors can be employed as functional redundant resistances when they are triggered in the active state. To decrease leakage power, the sleep transistors are turned off in sleep mode. A sleep transistor is known as a Header switch when it is connected to supply voltage, and as a Footer switch when it is connected to ground. The header power gating approach was employed in this project.

Flip-flops being essential components in sequential digital systems, but they consume a tremendous amount of chip area and power. Flip-flops are the fundamental building components of a sequential digital circuit. Because they have two stable states, logic low and logic high, flip-flops are also known as bi-stable circuits. Any triggering sets the circuit in one state, and any triggering change causes the flip-flop to switch states, necessitating the usage of a trigger pulse to change the state. In addition, clock signals are used as control inputs in flip flops. One bit is stored in each flip-flop.

Data Flip flop is represented by the block diagram below.

[1]*How to cite the article:*
Singh P., Shah P.K., Design of Power Gated True Single-Phase-Clocked Flip-Flop, IJRST, Jul-Sep 2022, Vol 12, Issue 3, 5-10, DOI: http://doi.org/10.37648/ijrst.v12i03.002

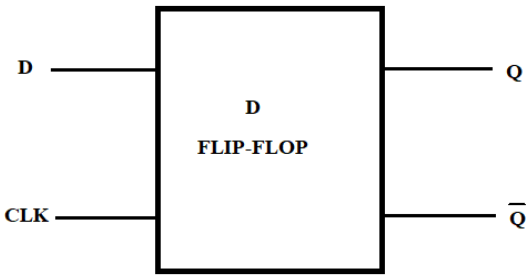

Fig.1 Data Flip-flop Block Diagram

Data Flip-flops are also found in data processors and memory storage elements. A D flip-flop can be built using either the NAND or the NOR gates. Because of their versatility, they are accessible as IC packages. A D flip-primary flop's functions include adding delay to a timing circuit, acting as a buffer, and sampling data at predefined intervals. D flip-flops feature a more straightforward electrical connection than JK flip-flops.

The input state has no impact on the resulting positioning only when clock signal is at its logic low. In order of the signals to function, the clock should always be configured to a large value. As a conclusion, the D flip-flop functions as a regulated Bi-stable latch that is controlled by the clock pulses. Positive and negative edge triggered D flip flops are available. As kind of a response, the outlet can continue to function in one of two stable states depending on the sources.

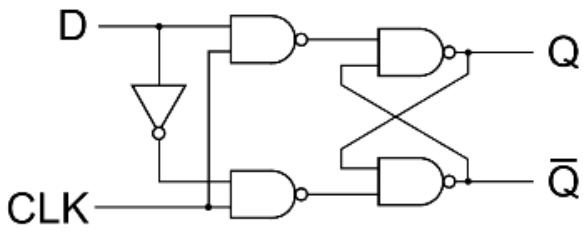

Fig.2 Conventional gate level architecture of D Flipflop

Table 1: D flipflop truth table

CLK	D	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	Q	$\bar{Q}$
1	0	0	1
1	1	1	0

From the above truth table, it can be observed that when the clk signal is high only, the data present in D input will be transferred to Q output.

Since the performance of Flip flops impacts the application, it is necessary to improve the performance of Flip flop.

RELATED WORKS

[13] Recommends a cross-charge control Flip Flop to lower charged gate capacitance and hence lessen power loss. As seen in Fig.3, XCFF's output terminal has a lot of current contention, therefore it's not ideal for low voltage usage. Further to that, regardless of the incoming information, XCFF must precharge certain inbuilt terminals, which wastes additional electricity.

The clock signal CK is low, whereas nodes X1 as well as X2 are precharged high. The data from an outlet NQ is stored in a slave latch. The node X1 is discharged lower only when clock CK grows or if the input signal D is high, leading an intermediate node M2 to advance and the out NQ to become lower. The output status is kept by a master latch when the CK is large. Once the clock CK rises and thus the input signal D falls below a certain threshold, the junction X2 is discharged lower and an out NQ rises. The node X1 would not alter if the input D hits level while the CK is high, because an internal node M1 gets too low only when node X2 drops.

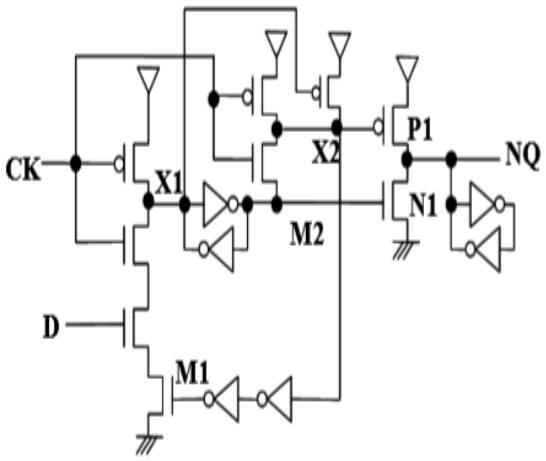

Fig.3: Schematic of XCFF

[16] Proposes a low-power single-phase-clocked combinational-type Flip-flop with an 18T single-phase clock. SPC-18T FF is made by rationalizing combinational logic in the same way as TCFF is made. Internal node F1 has repetitive precharge and discharge

procedures, as seen in Fig. 4, wasting a great deal of power.

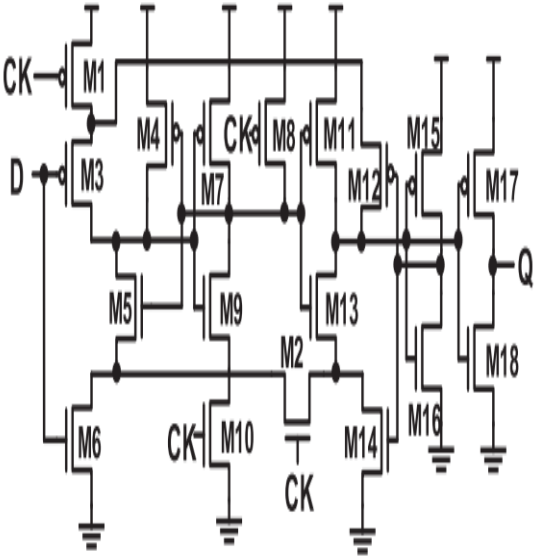

Fig.4: Schematic of SPC-18TFF

This technique proposes the use of a static single-phase-clocked contention-free Flip - flop (S2CFF). It is not appropriate for low voltages functioning because traditional TSPC FF is founded on dynamic logic and internal node voltages are not retentive. The internal node retentive issue is handled in S2CFF, allowing the FF to function properly at low supply voltage. The primary disadvantage of S2CFF is the waste of energy in duplicate precharge as well as discharge procedures.

The terminal net2 precharges towards VDD via M8 then discharges to GND via M9 as well as M10 somewhere at positive half cycle of CK after the data input remains at logic low level during the negative half cycle of CK. Because the output of the system is unaffected by the precharge as well as discharge processes, and also the node capacitance visible on the junction of net 2 is large, there is a significant amount of power wasted.

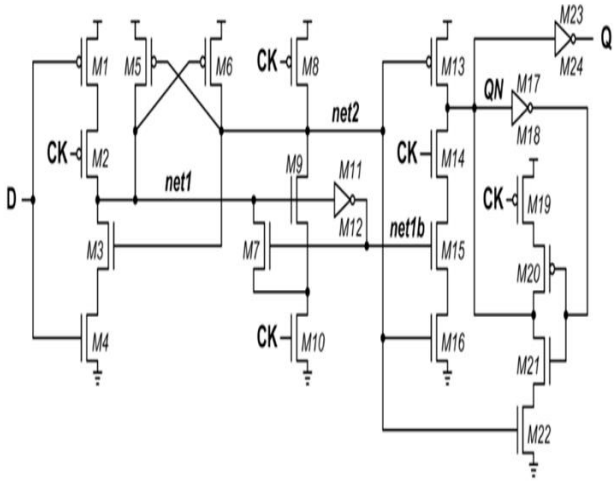

Fig.5: Traditional S^2CFF Flip flop.

The precharge channel should be cutoff whenever D = 0 to minimize the energy-wasting procedure. As seen in the Fig. 6, a PMOS M1 is introduced into the FF's precharge route and is regulated by the reversal of the input information. The PMOS M1 is turned on if the input signal is 1, and the appropriate precharge procedure is performed as regular. The PMOS M1 is turned off as the input information is kept zero, and the added transistor cuts off the precharge circuit. As a consequence, the precharge procedure is no longer superfluous.

The block diagram of fig.6 TSPC flip flop by eliminating the precharge scheme is shown below.

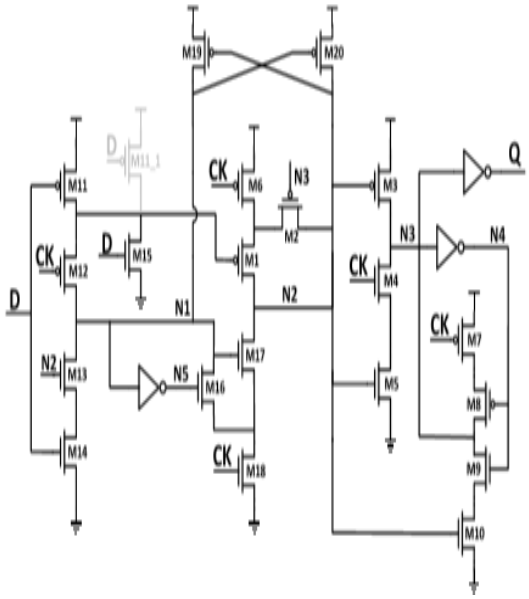

Fig.6. True single phase clock based flip flop

IMPLEMENTATION

Continuous production technology scaling improves chip efficiency and compactness, allowing many computations to be executed in less area. Electricity consumption, on the other hand, is rapidly increasing as technology progresses. Today's electronic devices, such as mobile phones and laptop computers, must have a high battery life. Heat is generated by power usage, necessitating the installation of costly cooling systems in servers and modern computer equipment. All of these reasons have forced designers to concentrate on low-power digital circuit design approaches.

Dynamic and static power consumption are two types of power consumption in digital circuitry. [3, 5]. Dynamic energy dissipation is caused by the charging / discharging of device as well as wiring capacitance. To avoid transistor breakdown due to high electric fields, new tech upgrading necessitates lowering the voltage levels. Supply voltage adjustment reduces the wastage of dynamic power, but at the expense of effectiveness. The threshold-old voltage must be changed to preserve reliability [6]. On the other side, lowering the threshold voltage causes higher leakage. Because the connection between threshold voltage and leakage is exponential, leakage power, also known as static power, is becoming a greater percentage of overall power consumption.

Flip flops are the basic Memory elements in many applications such as registers, counters which are mainly used in portable application. Hence low power consumption is need of the day. Leakage power consumption is a big concern because of technological scaling. To address this issue, the proposed TSPC Flip flop uses a header power gating mechanism. The power dissipation of the flip flop is minimized when this power gating technique is used since the power supply is turned off when it is not in use.

As future technologies expand and minimize power consumption, sub-threshold leakage currents will constitute a larger part of total power dissipation. One of its most successful leakage power reduction approaches is power gating. In this research, we offer a power gating technique for D-flip fop to minimize the power dissipation.

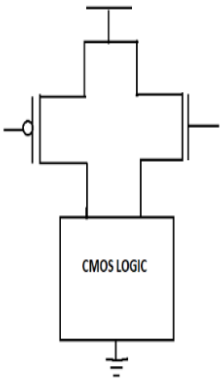

Fig.7: Block diagram of Power Gating

It can be observed from the fig.6 that when the gates of both pmos and nmos are on only the supply will be passed to the circuit.
The Schematic of power gated Tspc Flip-flop is shown below.

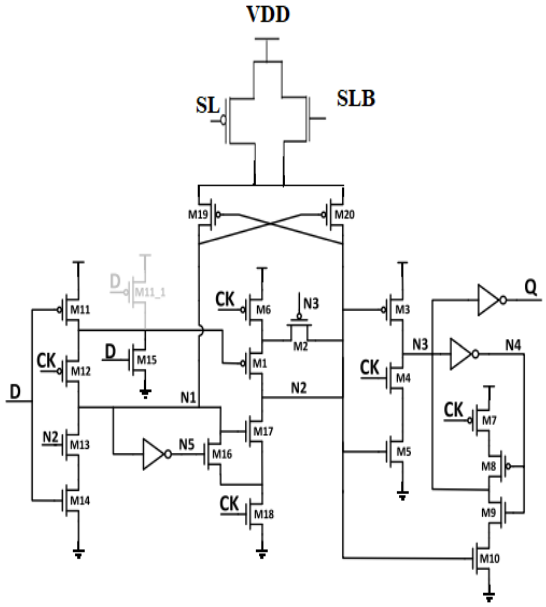

Fig.8: proposed power gated True single phase Flip-flop.

RESULTS AND DISCUSSIONS

The schematic diagram and waveform of power gated tspc based Flip-flop is shown below. Simulations are performed using Tanner EDA tool using 45nm technology.

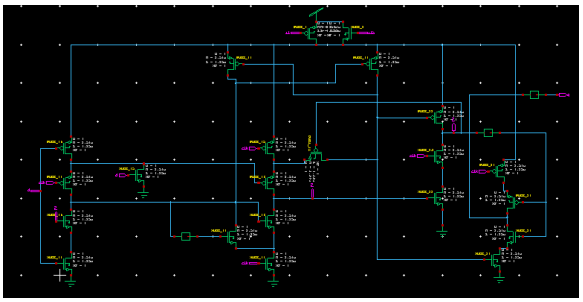

Fig.9 Schematic diagram of Proposed TSPC Flip flop

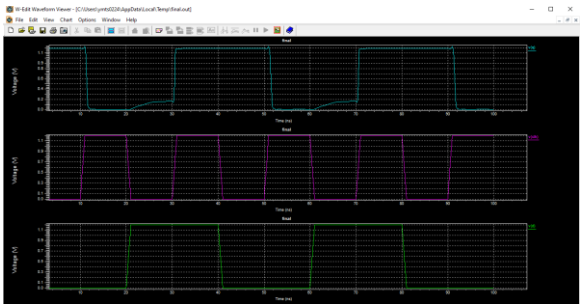

Fig.10: Waveform of proposed D –Flip flop

Table 2: Comparison table for Existing and Proposed methods

	Power (uw)	**Delay (ns)**	**Area**
Existing flip flop	1.874	0.19	26
Proposed flip flop	1.608	39.8	28

CONCLUSION

The design of power gated true single phase clock based flip-flops is presented in this article. Power gating is one of most widely technique for reducing consumption by shutting down the connection from the supply when not required. By applying the power gating concept, power consumption is minimized in the Suggested flip-flop design since the supply is passed to the circuit only when required in the proposed D flip-flop design.

REFERENCES

1. F. Chang et al., “Practical Strategies for Power-Efficient Computing Technologies”, Proceedings of the IEEE, Vol. 98, No. 2, pp. 215-236, 2010.
2. R. N. Agnes Shiny, B. Fahimunnisha, S. Akilandeswari and S. J. Venula, “Integration of Clock Gating and Power Gating in Digital Circuits”,2019 5th International Conference on Advanced Computing & Communication Systems (ICACCS), 2019, pp. 704-707.
3. S. M. Sharroush, “Impact of technology scaling on the performance of DRAMs”, 2016 5th International Conference on Electronic Devices, Systems and Applications (ICEDSA), 2016, pp. 1-4
4. M. Aguirre-Hernandez and M. Linares-Aranda, “A Clock-Gated Pulse-Triggered D Flip-Flop for Low-Power High-Performance VLSI Synchronous Systems”, 2006 International Caribbean Conference on Devices, Circuits and Systems, 2006, pp. 293-297.
5. B. Aparna and V. Anandi, “Design of a D flip flop for optimization of power dissipation using GDI technique”,2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), 2017, pp. 172-177.
6. N. Nedovic, M. Aleksic, and V. G. Oklobdzija, “Conditional techniques for small power consumption flip-flops”, in Proc. 8th IEEE Int. Conf. Electronics, Circuits Systems, Malta, Spain, Sept. 2–5, 2001, pp. 803–80.
7. Bonetti, A. Teman and A. Burg, “An overlap-contention free true-single-phase clock dual-edgetriggered flip-flop”, Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), pp. 1850-1853, May 2015.
8. A. Andrei, P. Eles, O. Jovanovic, M. Schmitz, J. Ogniewski, and Z. Peng, “Quasi-static voltage scaling for energy minimization with time constraints,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 1, pp. 10–23, Jan. 2011.
9. X. Zhang et al., “32bit×32bit multiprecision razor-based dynamic voltage scaling multiplier with operands scheduler,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 4, pp. 759–770, Apr. 2014.
10. W.-J. Tsou et al., “Digital low-dropout regulator with anti PVT-variation technique for dynamic voltage scaling and adaptive voltage scaling multicore processor,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2017, pp. 338–339.
11. S. Jain, L. Lin, and M. Alioto, “Dynamically adaptable pipeline for energy-efficient microarchitectures under wide voltage scaling,” IEEE J. Solid-State Circuits, vol. 53, no. 2, pp. 632–641, Feb. 2018.
12. J. Lee et al., “A self-tuning IoT processor using leakage-ratio measurement for energy-optimal operation,” IEEE J. Solid-State Circuits, vol. 55, no. 1, pp. 87–97, Jan. 2020.

13. A. Hirata, K. Nakanishi, M. Nozoe, and A. Miyoshi, "The cross charge control flip-flop: A low-power and high-speed flip-flop suitable for mobile application SoCs," in Dig. Tech. Papers. Symp. VLSI Circuits, Jun. 2005, pp. 306–307.
14. C. K. Teh, T. Fujita, H. Hara, and M. Hamada, "A 77% energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40 nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2011, pp. 338–339.
15. N. Kawai et al., "A fully static topologically-compressed 21-transistor flip-flop with 75% power saving," IEEE J. Solid-State Circuits, vol. 49, no. 11, pp. 2526–2533, Nov. 2014.
16. Y. Cai, A. Savanth, P. Prabhat, J. Myers, A. S. Weddell, and T. J. Kazmierski, "Ultra-low power 18-transistor fully static contentionfree single-phase clocked flip-flop in 65-nm CMOS," IEEE J. Solid-State Circuits, vol. 54, no. 2, pp. 550–559, Feb. 2019.
17. Y. Kim et al., "A static contention-free single-phase-clocked 24T flip flop in 45 nm for low-power applications," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2014, pp. 466–467.
18. F. Stas and D. Bol, "A 0.4-V 0.66-fJ/cycle retentive true-single-phaseclock 18T flip-flop in 28-nm fully-depleted SOI CMOS," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 3, pp. 935–945, Mar. 2018.
19. F. S. Alghareb, R. A. Ashraf, and R. F. DeMara, "Designing and evaluating redundancy-based soft-error masking on a continuum of energy versus robustness," IEEE Trans. Sustain. Comput., vol. 3, no. 3, pp. 139–152, Jul. 2018.
20. P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, and J. A. Felix, "Current and future challenges in radiation effects on CMOS electronics," IEEE Trans. Nucl. Sci., vol. 57, no. 4, pp. 1747–1763, Aug. 2010.
21. M. Fazeli, A. Patooghy, S. G. Miremadi, and A. Ejlali, "Feedback redundancy: A power efficient SEU-tolerant latch design for deep sub-micron technologies," in Proc. 37th Annu. IEEE/IFIP Int. Conf. Dependable Syst. Netw. (DSN), Jun. 2007, pp. 276–285.
22. Z. Huang, "A high performance SEU-tolerant latch for nanoscale CMOS technology," in Proc. Design, Automat. Test Eur. Conf. Exhib. (DATE), 2014, pp. 1–5.